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10/628,237	07/29/2003	Makoto Shizukuishi	107317-00060	4755

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EXAMINER	
TRAN, NHAN T	
ART UNIT	PAPER NUMBER
2622	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/628,237	SHIZUKUISHI, MAKOTO	
	Examiner	Art Unit	
	NHAN T. TRAN	2622	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 April 2008 and 31 January 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claims 1-19 have been considered but are moot in view of the new ground of rejection in view of the IDS references filed 1/31/2008.

Information Disclosure Statement

2. The information disclosure statement (IDS) submitted on 1/31/2008 is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ewedemi et al. (US 6,831,684) in view of Miyagawa Ryohei (JP 11-331709). *Note that these references cited in the IDS submitted by the Applicant on 1/31/2008.*

Regarding claim 1, Ewedemi discloses a solid state image pickup device (100 in Fig. 1) comprising:

a semiconductor substrate (semiconductor substrate of the integrated circuit) defining a two-dimensional surface (Fig. 1 and col. 2, lines 58-65);

a number of photoelectric conversion elements (pixels in pixel array 102) disposed in a light receiving area of said semiconductor substrate in a matrix shape and in a first number of rows and a second number of columns (Fig. 1 and col. 4, lines 55-60);

analog digital converters (each pixel has an A/D converter) in an area of said semiconductor substrate other than the light receiving area, said analog digital converters converting analog image data from said photoelectric conversion elements into digital image data (see col. 5, lines 1-13, and it is noted that the A/D converter for each pixel must be shielded from incident light to prevent noise and to maintain signal integrity by inherent design of an image sensor);

a memory (110 in Fig. 1) formed in an area of said semiconductor substrate other than the light receiving area at a succeeding stage of said analog digital converters, said memory having memory units, each corresponding to one of the photoelectric conversion elements, and recording the digital image data (see col. 5, lines 29-32 and col. 6, lines 39-45, wherein each digital pixel signal is stored in each 4-bit memory unit cell).

As disclosed above, Ewedemi teaches a plurality of A/D converters and each A/D converter is provided for each pixel. Ewedemi fails to teach that each A/D converter is provided for each column of pixels.

However, it is well recognized by Ryohei that the A/D conversion can be implemented by parallel column type A/D converters in which each A/D converter is corresponding to one column of pixels for converting analog signal into digital signal (see Ryohei, Fig. 1 and paragraph [0043]).

Therefore, it would have been obvious to one of ordinary skill in the art to modify the imaging device in Ewedemi to implement parallel column type A/D converters in which each A/D converter is corresponding to one column of photoelectric conversion elements in view of Ryohei instead of using each A/D converter for each pixel so as to reduce circuit size and cost of the imaging device.

Although Ewedemi and Ryohei disclose the memory (110 in Ewedemi) for storing digital image signal as discussed above, they do not explicitly disclose that the memory is a non-volatile memory. However, an Official Notice is taken that it is well known in the art to use a non-volatile memory that is made of one of NAND, NOR, floating gate, MONOS transistors or a ferroelectric memory for storing digital data since the non-volatile memory is able to retain data even when the power supply is lost.

Therefore, it would have been obvious to one of ordinary skill in the art to substitute the memory 110 in Ewedemi by a non-volatile memory so that the digital image data would be retained in the memory units in a case when the power supply was lost, thereby improving functionality and data security.

Regarding claim 2, as analyzed in claim 1, said non-volatile memory records the digital image data of one frame (see Ewedemi, col. 5, lines 29-32 in which the memory records *at least* one frame of digital image signals).

Regarding claim 3, it is also seen from col. 5, lines 29-32 of Ewedemi and the analysis of claim 1 that the non-volatile memory records the digital image data of a plurality of frames (this is met by at least one frame).

Regarding claim 4, since the digital data stored in the non-volatile memory (in place of memory 110) before outputting to another image processing module via bus 109 in a digital camera (col. 4, lines 51-67), the erasing means for erasing the digital image data after the digital image data stored in said non-volatile memory is read to an external device is inherent in such digital camera in order for the memory to store subsequent frames.

Regarding claim 5, as analyzed in claim 1 and disclosed by Ewedemi in col. 5, lines 29-32 and col. 6, lines 17-59, addresses of said non-volatile memory in a vertical direction are related to addresses of the light receiving area in the vertical direction (because the memory is capable of storing at least one frame of the digital image signals, the vertical addresses of the pixels and memory units must be related in order to properly store the image frame signals as disclosed).

Regarding claim 6, Ewedemi further discloses a data register (112 in Fig. 1) used in common for both data input (via bus 108) and output (via bus 107) for said non-volatile memory (see col. 7, lines 45-67).

Regarding claim 7, because the non-volatile memory as discussed in claims 1 and 2 is capable of storing at least one frame of the digital image signals output from the A/D converters, the non-volatile memory must have at least a depth of same bits (at least 4 bits) as output bits of said analog digital converters provided for each column (see Ewedemi, col. 5, lines 45-47).

Regarding claim 8, as analyzed in claim 1, the combined teaching of Ewedemi and Ryohei also discloses that each of said analog digital converters outputs the digital image data of one row of said photoelectric conversion elements in parallel, and said non-volatile memory records the digital image data of one row output parallel at a memory position corresponding to a row direction (see Ryohei in paragraph [0043] and Ewedemi in col. 5, line 29 - col. 6, line 59).

Regarding claims 9-13, these claims are also met by the analysis of claim 1, wherein the non-volatile memory can be made of one of NAND, NOR, floating gate, MONOS transistors or a ferroelectric memory.

Regarding claim 14, the combined teaching of Ewedemi and Ryohei as discussed in claim 1 further discloses a CCD for reading charges from said photoelectric conversion elements in the light receiving area and transfers analog image data to said analog digital converters provided for each column (see Ewedemi, col. 1, lines 42-46).

Regarding claim 15, the combined teaching of Ewedemi and Ryohei as discussed in claim 1 further discloses a MOS circuit for reading charges from said photoelectric conversion elements in the light receiving area and transfers analog image data to said analog digital converters provided for each column and wiring lines (see Ewedemi, col. 1, lines 42-46 and note that wiring lines are inherent for transferring data signal as disclosed).

Regarding claim 16, the combined teaching of Ewedemi and Ryohei further discloses a shutter control unit; and an optical system, and wherein said solid state image pickup device works as a digital camera (see Ewedemi, col. 4, lines 51-54, wherein the digital camera as disclosed by Ewedemi encompasses a shutter control unit and an optical system).

Regarding claim 17, it is also seen in claim 1 that the combined teaching of Ewedemi and Ryohei teaches that positions of said photoelectric conversion elements are identified by horizontal position and vertical position (pixel array 102 is identified as

NxM pixels as shown in Fig. 1 of Ewedemi), and said non-volatile memory units are identified by two dimensional addresses (x, y), x and y corresponding, respectively, to the horizontal and vertical positions of the photoelectric conversion element (see Ewedemi, col. 5, line 29 - col. 6, line 59 for the two dimensional memory that comprises x, y addresses corresponding to the x, y addresses of the pixel array for storing at least one full frame of image signals).

Regarding claim 18, it is also seen in the combined teaching of Ewedemi and Ryohei horizontal address decoder which decodes horizontal address of both the photoelectric conversion elements and the non-volatile memory units (see Fig. 1 of Ewedemi and Fig. 1 of Ryohei, wherein the horizontal address decoder is inherent in order for the imaging device to work properly).

Regarding claim 19, as analyzed in claim 1, the combined teaching of Ewedemi and Ryohei further discloses vertical address decoder including a scan circuit (VSR in Fig. 1 of Ryohei) which increments the vertical address (scanning row by row); wherein the vertical address decoder selects one of the photoelectric conversion elements rows (scanning row by row), to send analog image data thereof to the analog-digital converters, and send converted digital image data to corresponding non-volatile memory units (see Ryohei in paragraphs [0031-[0032] and [0043]-[0045] and Ewedemi, col. 5, line 29 – col. 6, line 59).

Conclusion

5. Applicant's submission of an information disclosure statement under 37 CFR 1.97(c) with the fee set forth in 37 CFR 1.17(p) on 1/31/2008 prompted the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 609.04(b). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to NHAN T. TRAN whose telephone number is (571)272-7371. The examiner can normally be reached on Monday - Friday, 8:00am - 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sinh Tran can be reached on (571) 272-7564. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Nhan T. Tran/
Primary Examiner, Art Unit 2622